Charles Eric LaForest, PhD

Email: eric.laforest@gmail.com
Web: https://fpgacpu.ca
Code: https://github.com/laforest/FPGADesignElements

Skills

- 17 years of experience with AMD/Xilinx/Intel/Altera Field-Programmable Gate Arrays (FPGA)
- 30 years of experience with Linux environments, both application and kernel programming
- Familiar with Verilog, VHDL, C/C++, Python, assembly (MIPS, ARM, 6502), Forth, etc...
- Custom hardware design for real-time control, high-speed interfaces, and data processing

Education

PhD, "High-Speed Soft-Processor Architecture for FPGA Overlays", University of Toronto, 2015

- Designed the Octavo multithreaded soft-processor (500 MHz on Stratix IV FPGA)
- Invented logic design techniques for early timing closure and parallel scaling

MASc, "Efficient Multi-Ported Memories for FPGAs", University of Toronto, 2009

- Reprinted 2012 as one of the top 25 papers of the first 20 years of the ACM FPGA conference

BIS, "Second-Generation Stack Computer Architecture", University of Waterloo, 2007

Diploma, Computer Engineering Technology, Algonquin College, Ottawa, 1999

Experience

FPGA Design Consultant, GateForge Consulting Ltd., Toronto, Apr 2016 – Present

- Custom floating-point complex-number linear algebra accelerator for real-time data processing
- Custom satellite 10 Gb/s optical sensor and DDR3 memory interfaces. Launched July 2024.
- High-precision (100+ bits) PID control with a custom Network-on-Chip (NoC)
- Ported Single Event Upset (SEU) test circuits from Virtex-5 to Virtex-7
- Implemented of space-rating test cases for defence-grade FPGA devices
- Debugged Closed Caption extraction from XDCAM video for a broadcasting platform
- Integrated video processing IP, ML acceleration, multiple DDR4 controllers, and multiple video encoding IPs on Virtex Ultrascale+ board, and wrote multi-core host-side control software
- Converted a set-top box video compositing product onto Amazon's F1 cloud FPGA platform
- Implemented audio and video format conversion and interfacing to H.264 encoding hardware

Principal Engineer, Summit Scientific Inc., Jan 2017 – Jun 2021

- Designed FPGA and software solutions for industrial, scientific, and medical applications
- Updated legacy EtherCAT interface to Linux and FreeRTOS Zynq platform
- Implemented FPGA interfaces to CPUs, DDR2 RAM, and a camera in a medical device

Senior ASIC/Layout Design Engineer, Advanced Micro Devices, Markham, Oct 2014 – Mar 2016

- Emulated AMD Secure Processor (PSP) on Xilinx Virtex 7 FPGA
- Led bring-up effort for post-silicon PSP diagnostic firmware
- Analyzed Synplify FPGA technology-mapping issues

Software Developer, Research In Motion, Waterloo, May – Aug 2006 and 2007

- Analyzed cross-core interface on multi-core mobile device to find performance bottlenecks
- Wrote new GSM regression test framework and test cases
- Debugged cellular modem software and interrupt handling

Research Assistant, University of Waterloo, May – Aug 2005
- Researched statistical detection of rhetorical choices (stylistic variations) in C source code

Shop Clerk, Capital Elevator Ltd, Ottawa, Feb 2003 – Sept 2004
- Managed the inventory, purchase, and B2B sales of elevator parts
- Designed and commissioned custom tools and parts
- Supplied the field mechanics and repaired electronic and mechanical parts in-shop

Electronics Instructor, Algonquin College, Ottawa, Jan - Apr 2003
- Taught a one-term Passive Circuits course. Designed and conducted lectures, tests, and labs.

Software Developer, TransGaming Technologies, Ottawa, Nov 2001 – Sep 2002
- Improved exception handling in PlayStation 2 Linux kernel for WIN32 emulation
- Implemented a credit card verification back-end for secure online membership purchases

Software Developer, Rebel.com, Ottawa, Jan 2000 – Sep 2001
- Researched adaptive fixed-point routines on ARM SA-110 CPU
- Designed an internal web-based package management database
- Managed the daily system image build for the NetWinder Linux distribution

Linux Consultant, OE/One, Ottawa, Jul – Dec 1999
- Implemented a PHP multimedia browser-based GUI with SQL database back-end
- Provided internal general Linux consulting services, computer installations, and tech support

Software Developer, Greylands/Zones Grises, Ottawa, Jun 1999
- Designed RS-232 Wi-Fi tunnel and binary floating-point conversion for mobile GPS units

Engineering Technologist, Applied AI Systems, Kanata, Feb – May 1999
- Assisted robot construction: research, procurement, machining, SMT PCB assembly
- Ported PID motor controller from proprietary Motorola 68000 platform to x86 Real-Time Linux
- Designed and implemented real-time software for IR, ultrasonic, and contact sensors

Publications

- Charles Eric LaForest and Jason Anderson. "Microarchitectural Comparison of the MXP and Octavo Soft-Processor FPGA Overlays". *ACM Transactions on Reconfigurable Technology and Systems (TRETS),* Volume 10, Issue 3, Article No. 19 (May 2017), 25 pages
- Charles Eric LaForest, Zimo Li, Tristan O'Rourke, Ming G. Liu, and J. Gregory Steffan. Composing Multi-Ported Memories on FPGAs. *ACM Transactions on Reconfigurable Technology and Systems (TRETS),* Volume 7, Issue 3, Article 16 (Sept. 2014), 23 pages.
- Charles Eric LaForest, Jason Anderson, and J. Gregory Steffan. "Approaching Overhead-Free Execution on FPGA Soft-Processors". *Proceedings of the IEEE International Conference on Field-Programmable Technology (ICFPT) 2014*, pp. 99-106
- Charles Eric LaForest, J. Gregory Steffan. Maximizing Speed and Density of Tiled FPGA Overlays via Partitioning. *Proceedings of ICFPT 2013*, pp. 238-245
  Charles Eric LaForest, Ming G. Liu, Emma Rae Rapati, and J. Gregory Steffan. Multi-Ported Memories for FPGAs via XOR. *Proceedings of the ACM International Symposium on Field-Programmable Gate Arrays (FPGA) 2012*, pp. 209-218
- Charles Eric LaForest, J. Gregory Steffan. Octavo: An FPGA-Centric Processor Family. *Proceedings of FPGA 2012*, pp. 219-228
- Charles Eric LaForest, J. Gregory Steffan. Efficient Multi-Ported Memories for FPGAs. *Proceedings of FPGA 2010*, pp. 41-50
  Awarded as one of the top 25 papers (top 5%) of the first 20 years of the conference. Reprinted in *FPGA20: Highlighting Significant Contributions from 20 Years of the International Symposium on Field-Programmable Gate Arrays (1992-2011).*

Miscellaneous: Amateur Radio Operator (Advanced License), Canadian Ski Marathon, 2000-2003